Time Interval Measurement Based on Fine-Time Synthesis Module

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***Abstract*—The time-to-digital converter (TDC) is a key technology for achieving accurate time delay measurements in fiber-optic time transmission and synchronization system. Current architectures for TDC implementation mainly consist of coarse counters paired with different fine counter architectures. Here, we propose and implement a new fine counter architecture that synthesizes the time interval between pulses and the reference clock into a single pulse. The width of synthesized pulse is measured to enhance precision through the reuse of measurement units. The TDC stability is evaluated through the back-to-back (BTB) experiment. The short-term time deviation (TDEV) is 8.07 ps@1s, and the long-term TDEV is 0.18 ps@10^4s. Additionally, the proposed TDC is applied in a laboratory-built round-trip time synchronization system over 680km fiber link. The timing jitter of the system is measured to be 38.02ps.**

***Keywords*—time-to-digital converter, fine time synthesis module, precision**

I. Introduction

The time-to-digital converter (TDC) represents a pivotal technology for the accurate measurement of time delays in fiber-optic time transmission and synchronization systems [1]. The current architectural approaches to TDC implementation primarily comprise coarse counters paired with distinct fine counter architectures [2]. These architectures include multi-phase clocked counters [3] and multi-chain parallel structures [4]. In the design of time interval measurement, the architecture of high precision fine counters has always been a concern of researchers. Here, we propose and implement a new fine counter architecture that synthesizes the time interval between pulses and the reference clock into a single pulse. The width of synthesized pulse is measured to enhance precision through the reuse of measurement units. This method improves the condition of stability degradation of the TDC chip used in the measurement unit when measuring larger orders of magnitude of time intervals. The TDC stability is evaluated through the BTB experiment. The short-term TDEV is 8.07 ps@1s, and the long-term TDEV is 0.18 ps@10^4s. Additionally, the proposed TDC is applied in a laboratory-built round-trip time synchronization system over 680km fiber link. The timing jitter of the system is measured to be 38.02ps.

II. Method

The principle of the fine time synthesis module is shown in Fig. 1(a). This paper proposes connecting the clock signal, start signal (ST), or stop signal (SP) through the different inputs of two D flip-flops to obtain the fine time signal. Fig. 1(b). depicts the diagram of overall system. The FPGA is responsible for the operation of the coarse counter, the control of several fine synthesis modules and the transmission of the test data. The clock manager consists of several parts, including phase-locked loop unit, clock fan-out unit, and inverter unit, which can provide 200MHz clock signals with different phases. The pulse width measurement is achieved by designing the peripheral circuits of the TDC-GPX2 (ScioSense) chip as a measurement unit. And the measurements of the fine time between ST/SP and different phases clocks improve the measurement precision through averaging. Due to the inherent build-up time limitation of the D-flip-flop, the measurement unit suffers from a dead zone problem caused by metastability. Clock signals with different phases in the TDC ensure that the other measurement unit is in a non-dead-zone range and that the TDC can obtain valid data.

III. Experiment

The TDC measures the fine time of the ST/SP signals using two measurement units respectively and averages the results. The stability of the TDC and the measurement units is evaluated through the experiment of measuring the time intervals of different magnitudes. Fig. 2(a). depicts the schematic diagram of the overall TDC system and GPX2 measurements with different time differences. The one pulse per second (1PPS) signals from the two channels of the pulse generator (Stanford Research Systems DG645) are used as ST/SP signals. Fig. 3. shows the TDEV of the TDC and the measurement unit for different time interval conditions. The TDEV of the measurement unit gradually increases as the magnitude of the time interval increases, and the TDEV of the TDC is smaller compared to the measurement unit under the same magnitude condition.

To further illustrate the stability of the TDC, The BTB experiment evaluates the stability of the TDC and the commercial time interval counter (Keysight 53230A). Fig. 2(b). depicts the schematic diagram of the BTB experiment with the overall TDC system and Keysight 53230A. The 1PPS from the pulse generator is divided and input into the ST and SP channels of TDC. We used this experimental setup to conduct an experiment lasting 5x10^4s. The measurement results are

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shown in Fig. 4. The short-term TDEV is 8.07 ps@1s, and the long-term TDEV is 0.18 ps@10^4s.

Additionally, the TDC is applied in a laboratory-built round-trip time synchronization system over 680km fiber link. In local site, the time signal is modulated by a phase modulator over an optical carrier with a wavelength of λ_L, and transmitted to remote site along fiber link. The transmitted signal is demodulation by Michelson interferometer and photodetector in remote side. And the 1PPS signal demodulated in remote site is transmitted back to the local site in the same manner except that the wavelength of optical carrier is λ_R. The TDC measures the time interval between the time signals generated by the local end and the time signal transmitted by the remote transmission of the local end. Based on the measurement of the time interval between round-trip signals, the delay time of the signals in the optical fiber is calculated from the before and after measurement data. Adjust the edge position of the ST signal of the DG645 at the local end to achieve the effect of compensating for the delay. The high-performance time measurement instrument (Carmel NK732) is used to evaluate the time interval between the time signal generated by the local terminal and the time signal demodulated by the remote site. The timing jitter of the system is measured to be 38.02ps.

IV. Conclusion

The TDC structure composed of FPGA coarse counters and fine time synthesis module has high precision and stability. Multiple-phase clock signals avoid the dead time problem of a single fine time synthesis module, and the stability of the measurement unit composed of TDC-GPX2 decreases when measuring different orders of magnitude of time intervals, and TDC improves the stability by multiplexing the measurement units. The BTB experiment shows that the measurement stability of this TDC structure is better than that of the Keysight 53230A and the TDC-GPX2 chip. In the short-term experiment of round-trip time synchronization system over 680km fiber link, the TIC using this TDC structure can realize a system with precision of tens of picoseconds.

References

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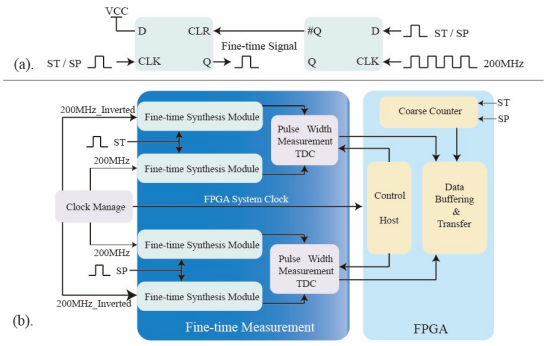

Fig. 1. (a). Principle of fine-time synthesis module. (b). diagram of overall system.

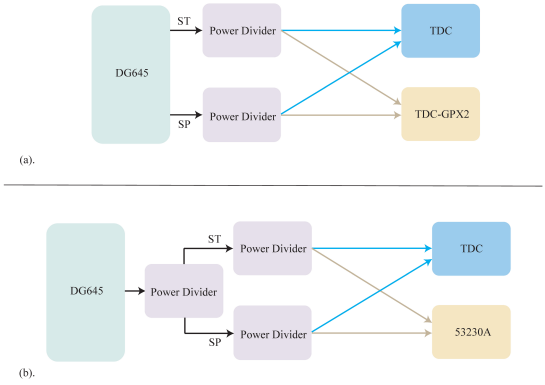

Fig. 2. (a). Schematic Diagram of the overall TDC system and GPX2 measurements with different time differences. (b). Schematic Diagram of the BTB experiment with the overall TDC system and Keysight 53230A.

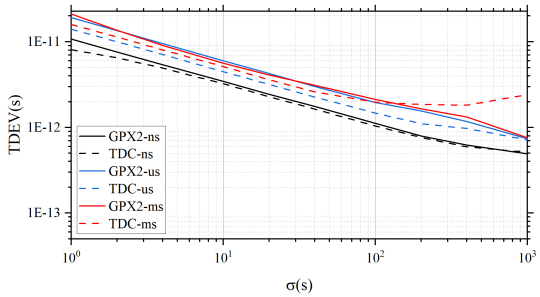

Fig. 3. TDC and GPX2 Measurement of TDEV at different magnitude time intervals.

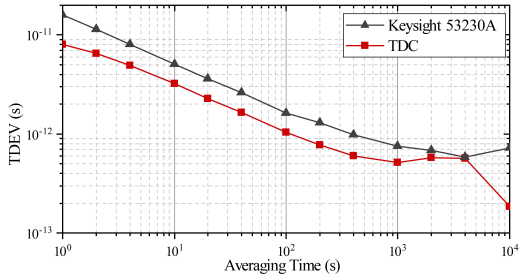

Fig. 4. The TDEV of TDC and Keysight 53230A.